Modelling and Predicting Memory Behavior in Parallel Systems with Network Links – Palladio-based Experiment Report
Symposium on Software Performance 2019

Philipp Gruber & Markus Frank
Motivation

Lewis
Software Engineer

Task: Ensure quality attributes

Reality:

Why?

Machine
100 Cores

Palladio (PCM)
• User
• Hardware
• Software

Performance prediction

Reality:

Linear speedup

Why?

[Frank16]
• RQ1 \(\rightarrow\) Is this possible?
• RQ2 \(\rightarrow\) Is it more accurate
Solution

• Modelling the memory bandwidth

How

• MemTest86 – RAM Benchmark → Throughput

• Model MemTest in Palladio
RQ1 → Is this possible?

Response time = Measurement

Solution
Solution

• Modelling the memory behavior

How

• Estimation model of miss/hit ratio

Ratio: 70:30

Lack in cache behavior information

Estimation model of miss/hit ratio

L1 → L2 → L3

Miss → Miss → Miss

Hit? → Done

Solution
Solution

- Measuring
- How
- Repetition of [Frank16]’s experiment
- Perf – Linux tool
- Plug in Palladio (repository model)

<table>
<thead>
<tr>
<th></th>
<th>1 Core</th>
<th>16 Core</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small (L3)</td>
<td>33:67</td>
<td>55:45</td>
</tr>
<tr>
<td>Small (L1)</td>
<td>75:25</td>
<td>70:30</td>
</tr>
</tbody>
</table>
Results
Results

Prediction error

![Bar chart showing prediction error for different M1 Cores. The chart compares prediction error with [Frank16] and Memory. The x-axis represents M1 Cores (2, 4, 8, 16) and the y-axis represents percentage (%). The prediction error values are as follows:

- For 2 Cores: [Frank16] = -7%, Memory = 11%
- For 4 Cores: [Frank16] = -7%, Memory = 11%
- For 8 Cores: [Frank16] = -5%, Memory = 17%
- For 16 Cores: [Frank16] = -33%, Memory = -7%

Legend:
- [Frank16] (Blue)
- Memory (Gray)
Results

Prediction error

<table>
<thead>
<tr>
<th>M2 - Cores</th>
<th>[Frank16]</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>-8</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>-21</td>
<td>-10</td>
</tr>
<tr>
<td>8</td>
<td>-23</td>
<td>-12</td>
</tr>
<tr>
<td>16</td>
<td>-20</td>
<td>-10</td>
</tr>
</tbody>
</table>

%
Summary

Lewis
Software Engineer

Task: Ensure Quality attributes

Machine
100 Cores

Reality:
Linear speedup
[Frank16]

Lessons learned:
• Proof of concept
• Accuracy gain
• Remaining inaccuracy

Future work:
• Hardware behavior
• Reduce the calibration effort
• Meta model changes
## Result

Measured cache ratios

<table>
<thead>
<tr>
<th></th>
<th>1 Core</th>
<th>2 Core</th>
<th>4 Core</th>
<th>8 Core</th>
<th>16 Core</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small (L3)</td>
<td>33:67</td>
<td>34:66</td>
<td>54:36</td>
<td>80:20</td>
<td>55:45</td>
</tr>
<tr>
<td>Small (L1)</td>
<td>75:25</td>
<td>75:25</td>
<td>75:25</td>
<td>75:25</td>
<td>70:30</td>
</tr>
<tr>
<td>Big (L3)</td>
<td>24:76</td>
<td>20:80</td>
<td>34:66</td>
<td>77:33</td>
<td>85:15</td>
</tr>
<tr>
<td>Big (L1)</td>
<td>70:30</td>
<td>70:30</td>
<td>70:30</td>
<td>70:30</td>
<td>70:30</td>
</tr>
</tbody>
</table>
Result

Prediction error

- 10% mean prediction error, before 15%

<table>
<thead>
<tr>
<th></th>
<th>2</th>
<th>4</th>
<th>8</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache L1-3</td>
<td>7.5</td>
<td>10.5</td>
<td>14.5</td>
<td>-8.5</td>
</tr>
<tr>
<td>Theory</td>
<td>3.5</td>
<td>26.5</td>
<td>99</td>
<td>150</td>
</tr>
<tr>
<td>replicas</td>
<td>-7.5</td>
<td>-14</td>
<td>-14</td>
<td>-26.5</td>
</tr>
</tbody>
</table>

→But …

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Matrix Multiplication

\[
\begin{pmatrix}
a_{11} & a_{12} & \cdots & a_{1k} \\
a_{21} & \cdots & \cdots & a_{2k} \\
\vdots & \vdots & \ddots & \vdots \\
a_{i1} & \cdots & \cdots & a_{ik}
\end{pmatrix}
\begin{pmatrix}
b_{11} & b_{12} & \cdots & b_{1j} \\
b_{21} & \cdots & \cdots & b_{2k} \\
\vdots & \vdots & \ddots & \vdots \\
b_{k1} & \cdots & \cdots & b_{kj}
\end{pmatrix}
\]

\[
\text{result}[i][j] = \text{result}[i][j] + \text{matrixA}[i][k] \times \text{matrixB}[k][j];
\]

Assumptions:

\(\rightarrow 1\) write \(\rightarrow 3\) read operations

\(\rightarrow 16\) Byte memory traffic per iteration \((3000\times3000\times3000)\)

\(\rightarrow 432\) GB overall
Cache measuring

Factors:
- Amount of modules
- L3 Size
- Clock frequency

Hardware „Potsdam“: 2*6 (2.5 GHz) vs. 4*10 (2.4 GHz)
- Cache: L1: 32 KB, L2: 256 KB, L3: 15 MB vs. 30 MB
- RAM: 24 GB vs. 896 GB

Factors: Amount of modules, L3 Size, Clock frequency
Speedup of the different experiments

![Graph showing speedup of different experiments with varying cores.](graph.png)
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References